3.　　(Amended) The <u>asynchronously-accessible</u> storage device of Claim 1, wherein the pipelined mode is an extended data out mode.

4.　　(Amended) The <u>asynchronously-accessible</u> storage device of Claim 1, wherein the burst mode is an extended data out mode.

5.　　(Amended) The <u>asynchronously-accessible</u> storage device of Claim 1, wherein the pipelined/burst mode circuitry includes a <u>buffer</u> [storage device], the <u>buffer</u> [storage device] for storing an address.

6.　　(Amended) The <u>asynchronously-accessible</u> storage device of Claim 5, wherein the pipelined/burst mode circuitry includes at least one counter for incrementing the address.

7.　　(Amended) The <u>asynchronously-accessible</u> storage device of Claim 1, wherein the pipelined/burst mode circuitry is coupled for receiving an external address.

8.　　(Amended) The [memory] <u>asynchronously-accessible storage</u> device of Claim 7, wherein the pipelined/burst mode circuitry includes a <u>buffer</u> [storage device] for storing the external address.

9.　　(Amended) The <u>asynchronously-accessible</u> storage device of Claim 7, wherein the pipelined/burst mode circuitry includes multiplexed devices for providing an internally generated address to the storage device.

33.　　(Amended) A method for accessing a storage device, [the method] comprising [steps of]:
　　　　receiving a first address to the storage device;
　　　　selecting between a burst <u>mode</u> and a pipelined mode of operation of the storage device;
　　　　selecting between outputting information from <u>the storage device</u> and inputting information to the storage device;
　　　　obtaining a second address to the storage device; [and]
　　　　accessing a storage element of the storage device using the first address and the second address; <u>and</u>
　　　　the storage device being asynchronously-accessible in either of the burst mode and the pipelined mode.

34.　　(Amended) [A method, as in] <u>The method of</u> Claim 33, further comprising [a step of] switching [as] between the burst mode and the pipelined mode.

35. (Amended) [A method, as in] The method of Claim 33, wherein the second address is an external address.

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46. (Amended) [Method] A method for accessing several different locations in an asynchronously-accessible memory device, [the method] comprising [steps of]:

selecting a [first] burst mode of operation;

providing a new external address for every access associated with asynchronously accessing the asynchronously-accessible memory device while in the [first] burst mode of operation;

switching modes to a [second] pipelined mode of operation;

providing an initial external address associated with asynchronously accessing the asynchronously-accessible memory device in the [second] pipelined mode of operation; and

generating at least one subsequent internal address patterned after the initial external address while in the [second] pipelined mode of operation.

In Claim 48, line 1, please delete "47", and insert therefor - - 46, - -.

In Claim 49, line 1, please delete "47", and insert therefor - - 46, - -.

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50. (Amended) A system comprising:

a microprocessor;

a memory, coupled to the microprocessor, for operating in burst or pipelined modes, wherein the memory is an asynchronous dynamic random access memory; and

a system clock coupled to the microprocessor[,]

[the memory not operating directly off the system clock].- -

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